AMENDMENT

In the claims:

Please replace claims 26 and 27 with the following amended versions of these claims.

26. (Three Times Amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

an interlevel dielectric disposed on the second conductive layer and including three insulating layers, two of the three insulating layers being separately planarized spin-on glass layers;

an insulating layer disposed on the interlevel dielectric; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

27. (Three Times Amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of separately planarized spin-on glass layers disposed on the second conductive layer;

an insulating layer disposed on a top one of the planarizing spin-on glass layers;

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches; and

wherein the plurality of separately planarized spin-on glass layers includes a first spin-on glass layer disposed on the second conductive layer, an oxide layer disposed on the first spin-on glass layer, and a second spin-on glass layer disposed on the oxide layer.